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Dual J-K Flip-Flops (with Preset and Clear)



ADE-205-423 (Z) 1st. Edition Sep. 2000

Description

Each flip-flop has independent J, K, preset, clear, and clock inputs and Q and \overline{Q} outputs. This device is edge-sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

Features

• High Speed Operation: t_{pd} (Clock to Q) = 21 ns typ ($C_L = 50 \text{ pF}$)

• High Output Current: Fanout of 10 LSTTL Loads

• Wide Operating Voltage: $V_{CC} = 2$ to 6 V

• Low Input Current: 1 μA max

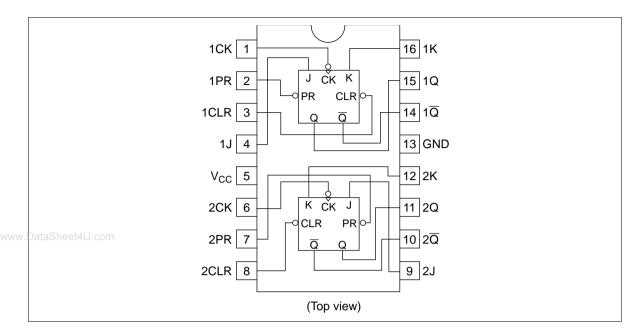
• Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max (Ta = 25°C)

Function Table

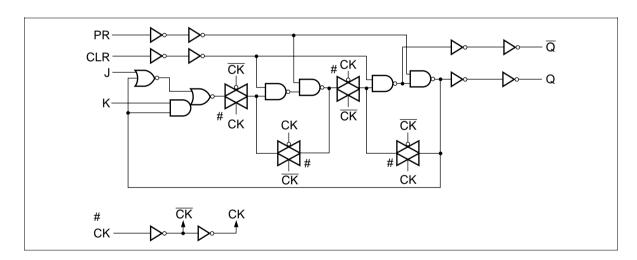
Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q
L	Н	Χ	Χ	X	Н	L
Н	L	Χ	Χ	X	L	Н
L	L	Х	Х	Х	H* ¹	H*1
Н	Н	_	L	L	No change	е
Н	Н	_	L	Н	L	Н
Н	Н		Н	L	Н	L
Н	Н	_	Н	Н	Toggle	
Н	Н	L	Х	Х	No change	е
Н	Н	Н	Х	Х	No change	е
Н	Н		Χ	Χ	No change	e

Note: 1. Q and \overline{Q} will remain HIGH as long as Preset and Clear are Low, but Q and \overline{Q} are unpredictable, if Preset and Clear go HIGH simultaneously.

Pin Arrangement



Block Diagram (1//2)



DC Characteristics

			Ta = 25°		= 25°C		Ta = -40 to +85°C			
Item	Symbol	V _{cc} (V)	Min	Тур	Max	Min	Max	Unit	Test Condition	าร
Input voltage	V _{IH}	2.0	1.5	_	_	1.5	_	V		
		4.5	3.15	_	_	3.15	_	-		
		6.0	4.2	_	_	4.2	_	-		
	V _{IL}	2.0	_	_	0.5	_	0.5	V		
		4.5	_	_	1.35	_	1.35	=		
		6.0	_	_	1.8	_	1.8	=		
Output voltage	V _{OH}	2.0	1.9	2.0	_	1.9	_	V	$Vin = V_{IH} or V_{IL}$	$I_{OH} = -20 \mu A$
.DataSheet4U.com		4.5	4.4	4.5	_	4.4	_	=		
		6.0	5.9	6.0	_	5.9	_	=		
		4.5	4.18	_	_	4.13	_	=		$I_{OH} = -4 \text{ mA}$
		6.0	5.68	_	_	5.63	_	=		$I_{OH} = -5.2 \text{ mA}$
	V _{OL}	2.0	_	0.0	0.1	_	0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$	I _{OL} = 20 μA
		4.5	_	0.0	0.1	_	0.1	=		
		6.0	_	0.0	0.1	_	0.1	-		
		4.5	_	_	0.26	_	0.33	=		I _{OL} = 4 mA
		6.0	_	_	0.26	_	0.33	-		I _{OL} = 5.2 mA
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	Vin = V _{CC} or GN	ND
Quiescent supply current	I _{cc}	6.0	_	_	2.0	_	20	μΑ	Vin = V _{CC} or GN	ND, lout = $0 \mu A$

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

4.5

6.0

2.0

4.5

6.0

2.0

4.5

6.0

2.0

4.5

6.0

 t_h

 t_{rem}

 $\boldsymbol{t}_{\text{TLH}}$

 t_{THL}

Cin

20 4

17

0

0

0

20

17

100 —

-3

-2

5

5

	Symbol	V _{cc} (V)	Ta = 25°C		+85°C				
Item			Min	Тур	Max	Min	Max	Unit	Test Conditions
Maximum clock	f _{max}	2.0	_	_	6	_	5	MHz	
frequency		4.5	_	_	30	_	24	_	
		6.0	_	_	35	_	28	=	
Propagation delay	t _{PLH}	2.0	_	_	150	_	190	ns	Clock to Q or Q
time	t_{PHL}	4.5	_	21	30	_	38	_	
		6.0	_	_	26	_	33	=	
		2.0	_	_	140	_	175	=	Clear to Q or Q
		4.5	_	17	28	_	35	_	
		6.0	_	_	24	_	30	_	
		2.0	_	_	140	_	175	_	Preset to Q or Q
		4.5	_	19	28	_	35		
		6.0	_	_	24	_	30	_	
Pulse width	t _w	2.0	80	_	_	100		ns	Preset, Clear, Clock
		4.5	16	6	_	20	_	_	
		6.0	14	_	_	17	_		
Setup time	t _{su}	2.0	100	_	_	125	_	ns	J or K to Clock

25

21

0

0

0

125

25

21

95

19

16

10

75

15

13

10

Clock to J or K

Preset or Clear to Clock

ns

ns

ns

pF

Hold time

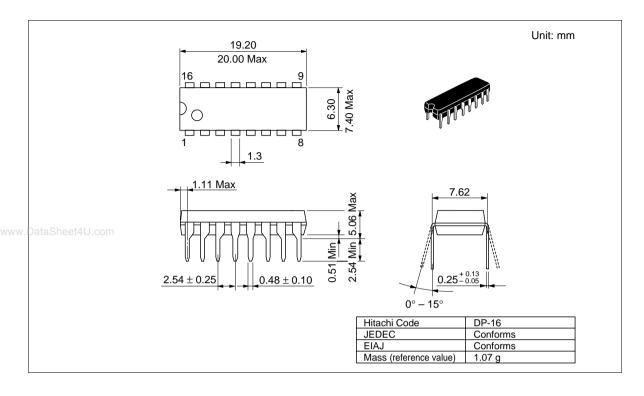
Removal time

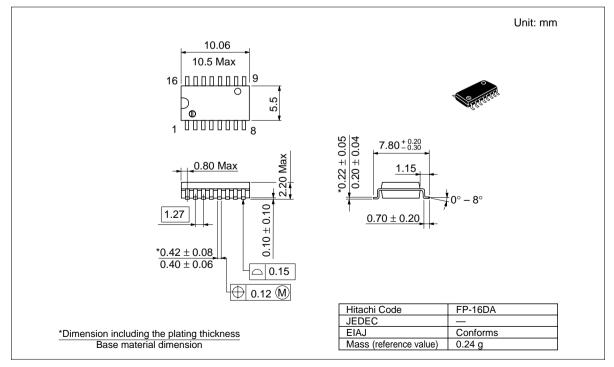
Output rise/fall

Input capacitance

time

Package Dimensions





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